

FIG. 1
(PRIOR ART)

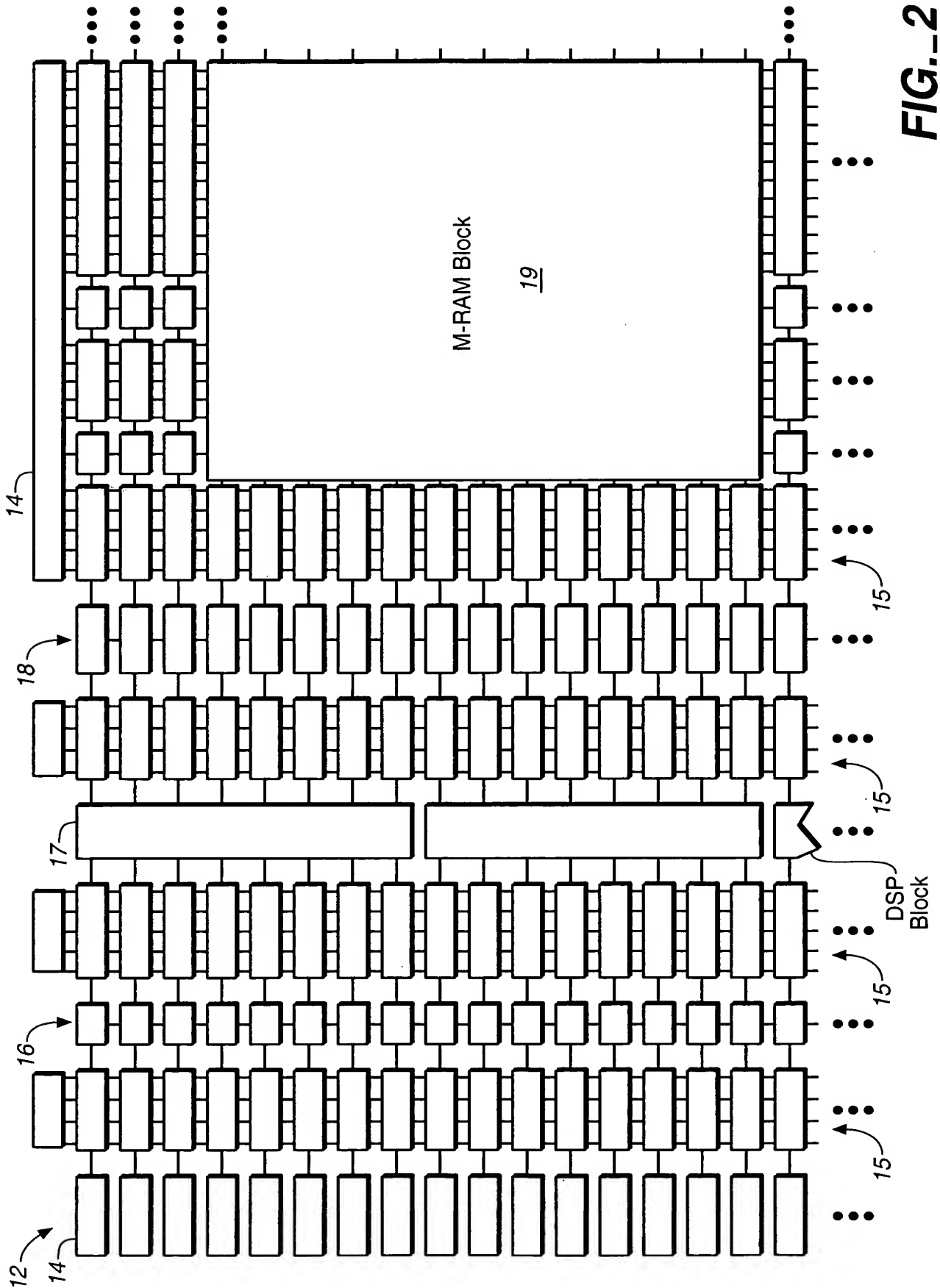


FIG. 2

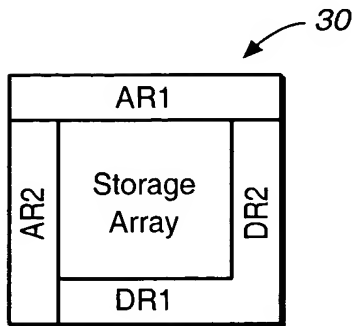


FIG._3

RAM Block Contents	
Address	Storage Contents
0000	0
0001	C0
0010	C1
0011	C0+C1
0100	C2
0101	C2+C0
0110	C2+C1
0111	C2+C1+C0
1000	C3
1001	C3+C0
1010	C3+C1
1011	C3+C1+C0
1100	C3+C2
1101	C3+C2+C0
1110	C3+C2+C1
1111	C3+C2+C1+C0

FIG._5

TABLE I

RAM Block Contents	
Address	Storage Contents
0000	0
0001	D0
0010	D1
0011	D0+D1
0100	D2
0101	D2+D0
0110	D2+D1
0111	D2+D1+D0
1000	D3
1001	D3+D0
1010	D3+D1
1011	D3+D1+D0
1100	D3+D2
1101	D3+D2+D0
1110	D3+D2+D1
1111	D3+D2+D1+D0

TABLE II

RAM Block Contents	
Address	Storage Contents
0000	0
0001	F0
0010	F1
0011	F0+F1
0100	F2
0101	F2+F0
0110	F2+F1
0111	F2+F1+F0
1000	F3
1001	F3+F0
1010	F3+F1
1011	F3+F1+F0
1100	F3+F2
1101	F3+F2+F0
1110	F3+F2+F1
1111	F3+F2+F1+F0

FIG._6

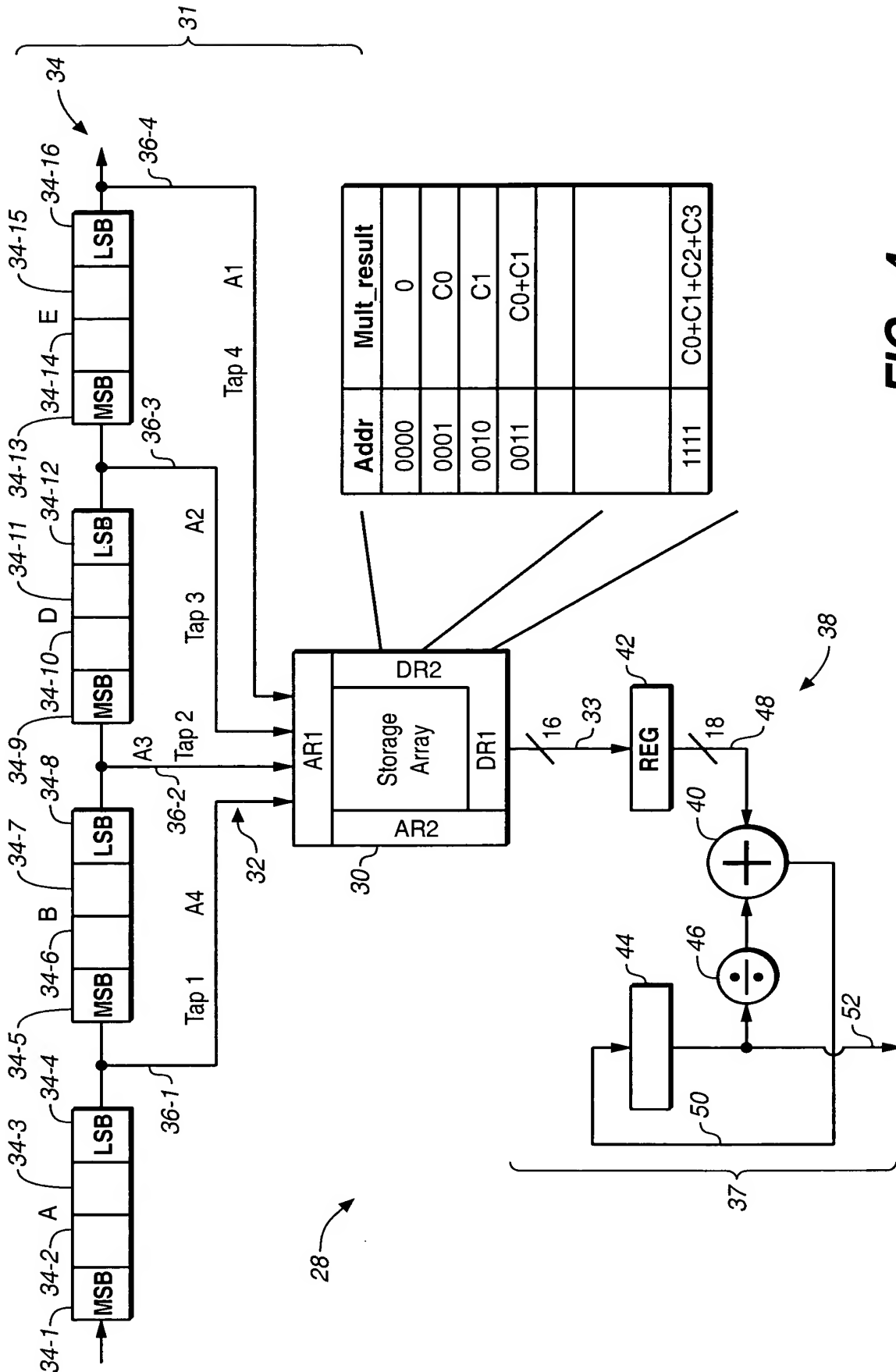


FIG. 4

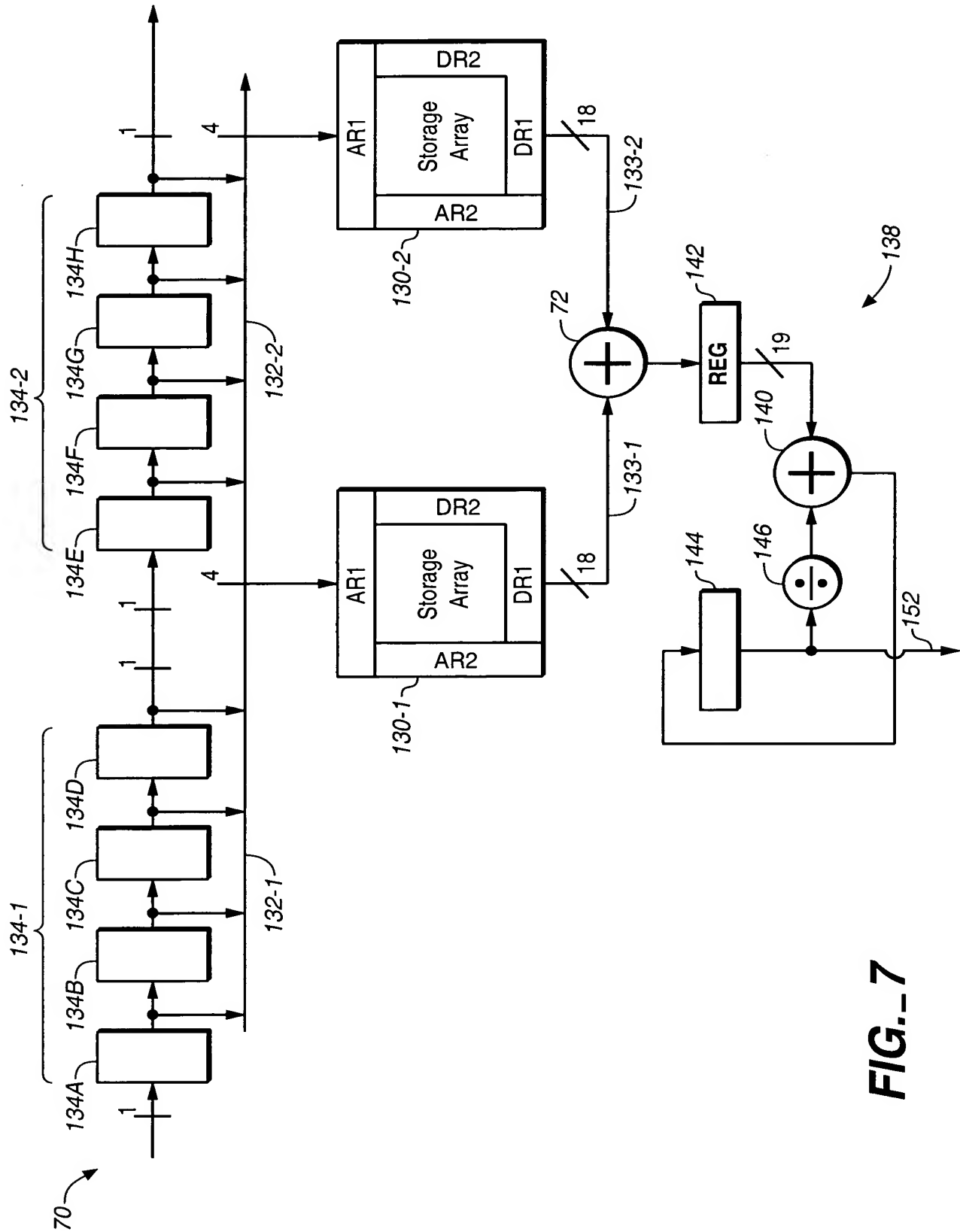


FIG. 7

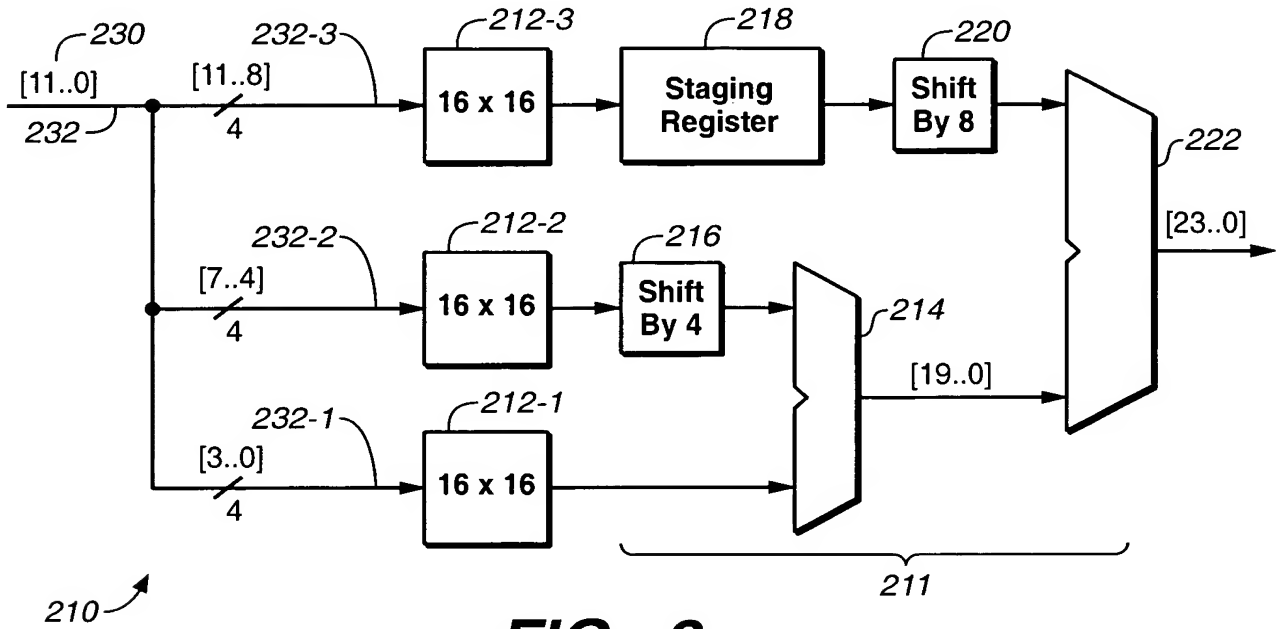


FIG. 8

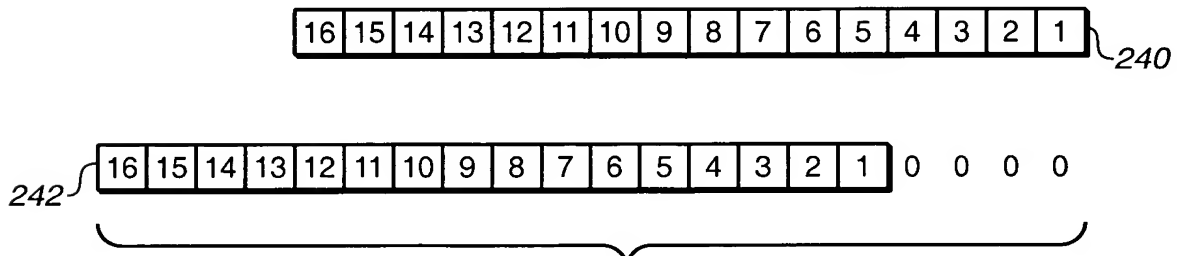
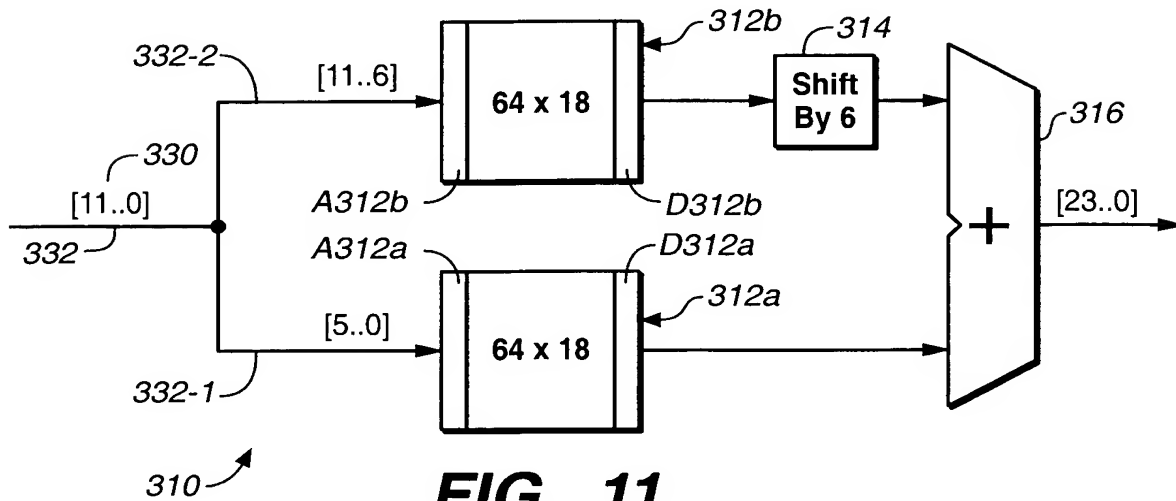


FIG. 9

Address	Multiplication Result
0000	0
0001	C
0010	2C
0011	3C
0100	4C
...	...
1111	15C

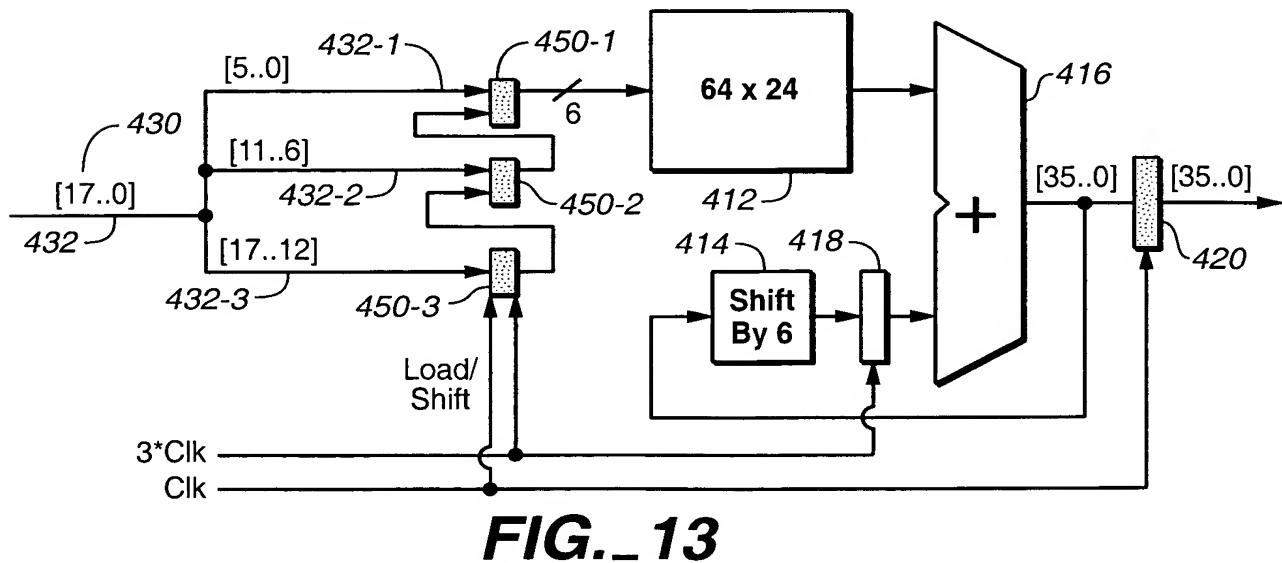
FIG. 10

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Address	Multiplication Result	Address	Multiplication Result
000000	0	000000	0
000001	Ca	000001	C
000010	2Ca	000010	2Cb
000011	3Ca	000011	3Cb
000100	4Ca	000100	4Cb
...
111110	62Ca	111110	62Cb
111111	63Ca	111111	63Cb

FIG. 12



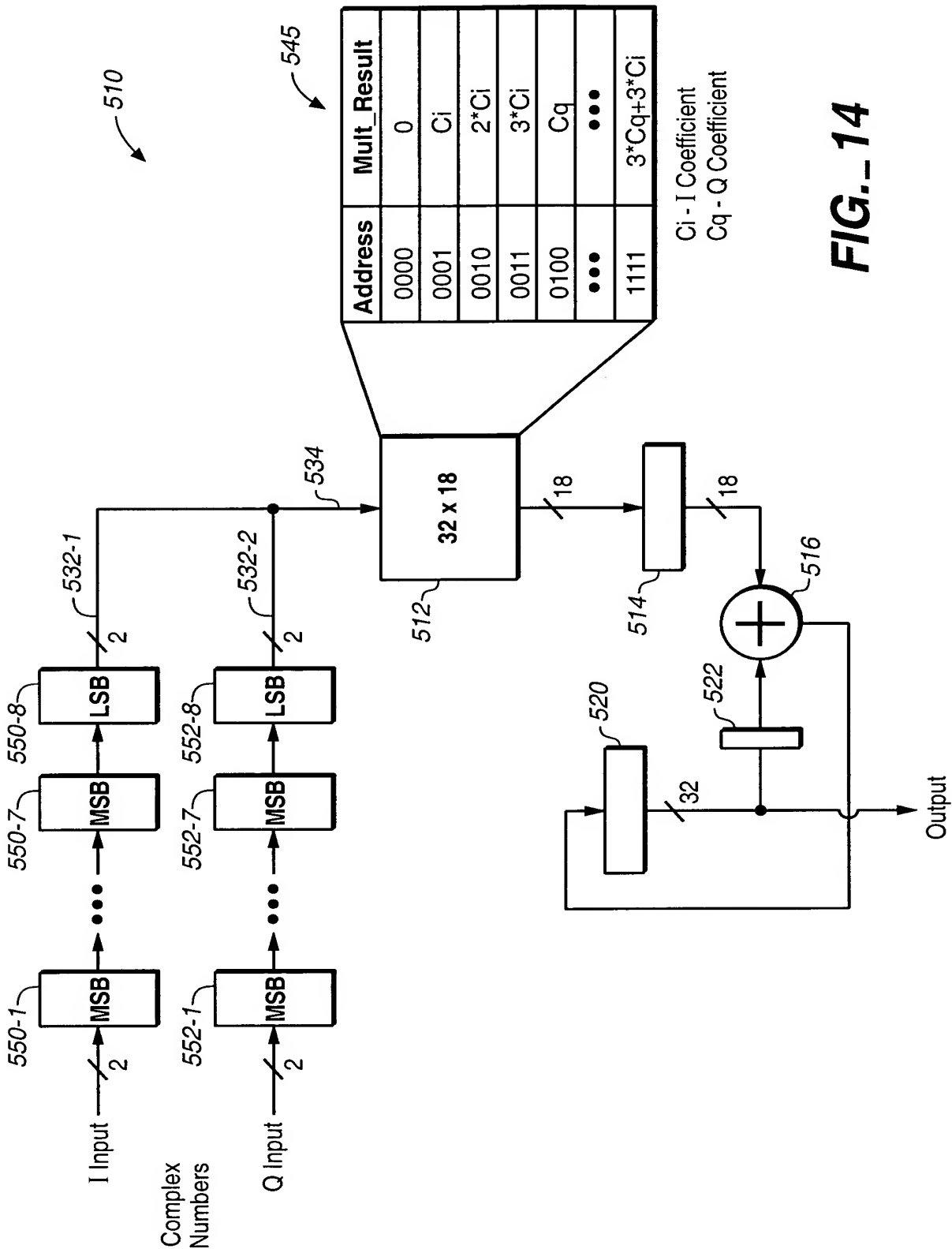


FIG. 14